Instruction:

Complete all questions in 1 hour.

1. Which one is the characteristic of Harvard Architecture?

# Program and Data stored in Separate Memory

* 1. Program and Data stored in the same Memory
  2. Program and data stored in Cache Memory
  3. All of the Above

1. Which of the following is the working cycle of the CPU?
   1. Decode, Execute, Fetch

# Fetch, Decode, Execute

* 1. Fetch, Execute, Decode
  2. All of the Above

1. Any condition that causes a processor to stall is called

# Hazard

* 1. Page fault
  2. System error
  3. None of the mentioned

1. What does the control unit generate to control other units?
   1. Transfer signals
   2. Command Signal

# Control signals

* 1. Timing signals

1. What must the processors of all computers have?
   1. Control unit
   2. ALU
   3. Register

# All of these

1. Which is the fastest memory in the computer?
   1. Cache
   2. RAM

# Register

* 1. Hard disk

1. With the help of , we reduce the memory access time:
   1. SDRAM

# Cache

* 1. Heaps
  2. Higher capacity RAMs

1. For a given FINITE number of instructions to be executed, which architecture of the processor provides for a faster execution?
   1. ISA
   2. ANSA

# Super-scalar

* 1. All of the mentioned

1. A processor performing fetch or decoding of different instruction during the execution of another instruction is called
   1. Super-scaling

# Pipe-lining

* 1. Parallel Computation
  2. None of the mentioned

1. A 24 bit address generates an address space of locations. A. 1024

B. 4096

C. 248

# D. 16,777,216

1. The USA contains about 3100 counties. Suppose you have a table that stores, for each county, its name (up to 40 characters in 8-bit ASCII), its state (a two-letter code), its population, and its median income (both as 32-bit numbers). How much space would the whole database take in memory?

Name=40\*8 State=2\*8 Population=32 Median=32 Now,

For 1 county=400

Then,Total space in databyte=400\*3100

=12,40,000 bits

=(12,40,000/8)/1024 KB In KB =151.367 KB

1. The computer has a maximum addressable memory of 16 Gigabytes. Its address bus width is 32.
2. Calculate the width of the data bus.

Total memory=2^address bus \* width of data bus 16\*2^30 =2^32 \* width of data bus

2^4\*2^30\*2^3 =2^32 \* width of data bus width of data bus =32=4 bits

1. State the effect that adding one new line to the address bus would have on the maximum addressable memory.

Total memory=2^(32+1) \* 4

=2^35

=2^5 \* 2^30

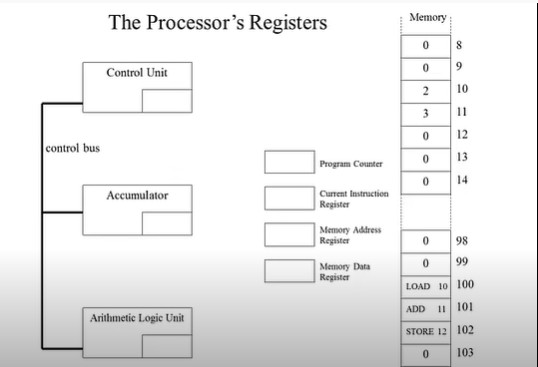
= 32 GB

1. Explain the *Instruction cycle* of the processor by taking an example of the program

Load: [10]

Add : [11]

Store: [12]



Upon the first instruction, the processor retrieves the instruction from memory. For example, in the above program, the processor would fetch the instruction "Load: [10]". Then, since the instruction Load: [10] is addressed as 100, the Program Counter will store 100. So will the Memory Address Register. And the Current Instruction Register and Memory Data Register will store the instruction "Load: [10]" as it is. Then the Control Unit will store 2 and transfer it to the Accumulator since 10 is stored as 2 in the memory. Then the Program Counter will be changed to 101 automatically which will be followed by the MAR. After this, 101 is addressed as ADD11. The CIR and MDR store the instruction “ADD 11” as it is. Then CU will fetch 3 as 11 is stored as 3 in memory then it is transferred to Accumulator. After this the value will be to 102 in PC and MAR will change to 102 as well. Then the CIR and MDR store instructions as “Store 12”. Since 12 is set as 5 in the memory. After this the stored values in Accumulator will transfer it to ALU where 2 and 3 will be added and the output will be 5. After the calculation, the output will be transferred again to the Accumulator.

1. Write short notes on the following topic:

Von Neumann and Harvard Architecture

The Von Neumann architecture, also known as the Von Neumann model or the Princeton architecture, is a computer architecture that stores both instructions and data in a single memory area. John von Neumann, a mathematician, created this architecture in 1945, and it has since become the most prevalent design for general-purpose computers.

Harvard architecture is a computer architecture that separates instruction and data memory and allows both to be accessed simultaneously. This design was developed in the 1980s at Harvard University and is utilized in many embedded devices and microcontrollers today.

RISC vs CISC architecture

Reduced Instruction Set Computing (RISC) is a computer architecture that employs a small number of general and basic instructions that can be executed quickly. RISC architectures are intended to maximize performance by lowering instruction set complexity and employing a smaller number of instructions.

Complicated Instruction Set Computing (CISC) is a computer architecture that employs a larger and more complex instruction set to execute a greater range of activities. CISC designs are intended to be more adaptable and capable of handling a larger range of jobs, however they may be slower than RISC systems.